REMARKS

Favorable reconsideration of this application, in light of the following remarks, is respectfully requested.

Claims 1-21 are pending in the current application. Of those, claims 1, 7, 10, and 20 are independent claims. No claims have been amended or canceled by this Response.

Claim Rejection – 35 U.S.C. § 112

Claims 1-5 and 7-20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant respectfully traverses this rejection for the reasons given below.

The Examiner has maintained that the term "processor" is not clearly defined in the specification. Applicants respectfully disagree and submit that the term "processor" as defined in the specification is clear, concise and exact and that one of ordinary skill in the art would clearly recognize the meaning of the term in light of the example embodiment illustrated in FIG. 2, for example, and as described in the specification. Applicant respectfully submits that one skilled in the art would also recognize from the description of the processor 200 in example embodiments in the specification, in particular, the inclusion of a processor core and/or a peripheral device within the processor 200, that a processor according to example embodiments may be interpreted more broadly than what the Examiner might consider a more traditional definition of a processor. Accordingly, the specification enables any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention as required by 35 U.S.C. § 112, first paragraph.

In view of the above, Applicant respectfully requests the rejections under 35 U.S.C. § 112 be withdrawn.

Claim Rejections – 35 U.S.C. § 102

Claims 1-21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,475,324 to Tomiyori ("*Tomiyori*"). Applicant respectfully traverses this rejection for the reasons given below.

Claim 1 recites a processor having a processor core and at least one peripheral device, comprising, *inter alia*, a selecting circuit for ***determining* at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit** based on direct monitoring of the high-speed control circuit and the low-speed and low-power control circuit and for outputting a selection signal based on the determination. (Emphasis Added)

The Examiner asserts "a selecting circuit" of claim 1 upon clock switching circuit 30 and clock control circuit 60 of FIG. 1 of *Tomiyori*, "a high-speed control circuit" of claim 1 upon clock generation circuit 10, oscillator 11 and frequency count circuit 40 of FIG. 1 of *Tomiyori* and "a low-speed and low-power control circuit" of claim 1 upon clock generation circuit 20, oscillator 21 and frequency count circuit 40 of FIG. 1 of *Tomiyori*.[1]

However, *Tomiyori* discloses that the frequency count circuit 40 counts the frequency of the second clock CLK2 using the first clock CLK1 as reference.[2] A clock control circuit 60 controls the clock switching circuit 30 based on the frequency data sent from the frequency count circuit 40. The clock control circuit 60 of *Tomiyori* determines the stability of the second clock CLK2 based on the frequency count signal 102 sent from the frequency count circuit 40.[3] As such, the clock control circuit 60 of *Tomiyori* does not determine the operating frequency of the first clock CLK1 or the second clock CLK2, let alone the operation states of the first clock CLK1 or the second clock CLK2. Accordingly, *Tomiyori* fails to teach or fairly

[1] Office Action, Page 3, Lines 1-6
[2] *Tomiyori*, Abstract and Column 4, Lines 40-42
[3] *Id.*, Column 4, Lines 53-56

suggest "a selecting circuit for **determining at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit** based on direct monitoring of the high-speed control circuit and the low-speed and low-power control circuit and for outputting a selection signal based on the determination," as required by independent claim 1. (Emphasis Added)

With regard to independent claims 7, 10 and 20, although claims 7, 10 and 20 should be interpreted based solely upon the limitations present therein, they are allowable for at least reasons somewhat similar to those set forth with regard to claim 1.

Claims 2-6, 8-9, 11-12 and 21, dependent on one of independent claims 1, 7, 10 and 21, are patentable for the reasons stated above with respect to claims 1, 7, 10 and 21 as well as for their own merits.

Applicant notes that the Examiner has failed to apply any art grounds of rejection to claims 13-19. Applicant respectfully submits that claims 13-19, dependent on independent claim 10, are also allowable for at least the reasons stated above with respect to claim 10 as well as for their own merits.

Applicant respectfully requests that the rejections of claims 1-21 under 35 U.S.C. § 102(b) be withdrawn.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of the claims in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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